

Numerical simulation of the response of substrate traps to a voltage applied to the gate of a gallium arsenide field effect transistor

N. Sengouga a,n, Af.Meftah a, Am.Meftah a, M.Henini b a

Laboratoire des Matériaux Semiconducteurs et Métalliques (LMSM), Université de Biskra,
BP145, 07000 Biskra, Algeria b School
of Physics and Astronomy, Nottingham Nanotechnology and Nanoscience Center, University
of Nottingham, Nottingham, NG72RD, UK

Abstract

We report on a numerical simulation of the response of substrate traps to a voltage applied to the gate of a gallium arsenide field effect transistor (GaAs FET) using proprietary simulation software. The substrate is assumed to contain shallow acceptors compensated by deep levels. The ratio between the densities of deep and shallow levels is considered to be one hundred, which is a typical value for semi-insulating substrates.

Although several traps may be present in the substrate but only the most commonly observed ones are considered, namely hole traps related to Cu and Cr, and the familiar native electron trap EL2. The current-voltage characteristics of the GaAs FET are calculated in the absence as well as in the presence of the above mentioned traps. It was found that the hole traps are affected by the gate voltage while the electron traps are not. This effect on the response of hole traps is explained by the fact that the quasi-hole Fermi level in the substrate is dependent on the gate voltage. However, the electron quasi-Fermi level in the substrate is insensitive to the gate voltage and therefore electron traps are not perturbed.

Keywords:

Substrate traps Gate voltage GaAs MESFET SILVACO simulation